TRANSISTOR WITH REDUCED GATE-TO-SOURCE CAPACITANCE AND METHOD THEREFOR

ABSTRACT

A power transistor, formed from transistors connected in parallel, each transistor is formed in an active region using a relatively long gate called a gate finger that is typically formed from polysilicon that accumulates resistance over its length. To alleviate this, the gate finger is strapped to a metal line at tabs adjacent to the finger gate over the active area, typically over the source, but the tabs add gate-to-source capacitance. This was previously quite small but as gate dielectrics have gotten thinner there is more capacitive coupling to the substrate by the tabs, and as gates have gotten thinner there is more resistance in the polysilicon finger gates. Both have the effect of increasing the RC time constant of the gate finger. This increase in RC time constant is alleviated by increasing the thickness of the dielectric separating the tabs from the substrate thereby reducing the capacitance caused by the tabs.